REMARKS/ARGUMENTS

Reconsideration of the present application is politely requested. Claims 1-17 remain active in the case. In order to more particularly point out and distinct claim that which the applicant regards as his invention, claims 1 and 9 have been amended. No new matter in introduced by this amendment.

1. Rejections over claims 1-8:

Claim 1 was rejected under 35 U.S.C. 102(b), for reasons of record that can be found on pages 2-3 in the Office action identified above, which is Part of Paper No./Mail Date 070521. Claim 1 was rejected by the Examiner because of Lee et al. (US 6,486,059 B2). The applicant notices that Lee et al. (US 6,486,059 B2) has been assigned to the same party of the present application.

Lee et al. teaches a dual damascene process using an oxide liner 52 for a dielectric barrier layer. The oxide liner 52 is formed on sidewalls of a dual damascene opening 50 that is created in a first and second low-k dielectric layers. To reduce resistance, a copper reduction step (col. 4, lines 3-10) is required to remove oxide from the exposed surface of the bottom wiring 32. A metal barrier layer 54 is then conformally deposited on interior surface of the dual damascene opening. A degas step is performed after the formation of the oxide liner.

The applicant submits that the degas step taught by Lee is different from the annealing step as required by the amended claim 1. After the formation of the oxide liner and the copper reduction step, the via hole and trench of the dual damascene opening are filled with outgas, which may include water vapor or byproducts. The purpose of the degas step taught by Lee et al. is to remove these water vapor or byproducts (outgas) out of the dual damascene opening, rather than from the inside of the first and second low-k dielectric layers.

To improve the quality of the deposited barrier layer, the claimed invention uses a step of annealing to remove the gas substances trapped in voids of the low-k dielectric layers. The claimed invention does not require the step of forming an oxide liner and also the step of reducing copper, thus the manufacture cost can be reduced.

It is respectfully suggested that, in light of the above, none of the cited references, alone or in combination, teaches or makes obvious all of the limitations of the amended claim 1. Reconsideration of claim 1 is therefore politely requested. As Claims 2-8 are dependent upon claim 1, they should be allowable if claim 1 is allowed. Reconsideration of claims 2-8 is therefore politely requested.

2. Rejections over claims 9-17:

Claim 9 was rejected under 35 U.S.C. 103(a), for reasons of record that can be found on pages 4-9 in the Office action identified above, which is Part of Paper No./Mail Date 070521. Claim 9 was rejected by the Examiner because of Lee et al. (US 6,486,059 B2). The applicant notices that Lee et al. (US 6,486,059 B2) has been assigned to the same party of the present application.

Lee et al. teaches a dual damascene process using an oxide liner 52 for a dielectric barrier layer. The oxide liner 52 is formed on sidewalls of a dual damascene opening 50 that is created in a first and second low-k dielectric layers. To reduce resistance, a copper reduction step (col. 4, lines 3-10) is required to remove oxide from the exposed surface of the bottom wiring 32. A metal barrier layer 54 is then conformally deposited on interior surface of the dual damascene opening. A degas step is performed after the formation of the oxide liner.

The applicant submits that the degas step taught by Lee is different from the annealing step as required by the amended claim 9. After the formation of the oxide liner and the copper reduction step, the via hole and trench of the dual damascene opening are filled with outgas, which may include water vapor or byproducts. The purpose of the

degas step taught by Lee et al. is to remove these water vapor or byproducts (outgas) out of the dual damascene opening, rather than from the inside of the first and second low-k dielectric layers. In other words, the aforesaid outgas to be removed by the degas step is not contained by the low-k dielectric layers according to Lee.

To improve the quality of the deposited barrier layer, the claimed invention uses a step of annealing to remove the gas substances trapped in voids of the low-k dielectric layers. The claimed invention does not include the step of forming an oxide liner and also the step of reducing copper, thus the manufacture cost can be reduced.

It is respectfully suggested that, in light of the above, none of the cited references, alone or in combination, teaches or makes obvious all of the limitations of the amended claim 9. Reconsideration of claim 9 is therefore politely requested. As Claims 10-17 are dependent upon claim 9, they should be allowable if claim 9 is allowed. Reconsideration of claims 10-17 is therefore politely requested. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

Winston Hsu

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)